The ARGO Approach: Parallelization Toolchain for Model-based Real Time Applications

**Objective:** WCET-aware User-Interactive Software Parallelization and Code Generation of Real-Time Software starting from High-Level Applications

### The ARGO Approach

- **Scalability up to 100 using multiple cores**
- **Horizon 2020 research and Start Date/Duration**
- **Maximizing worst-core architectures**
- **Predictable multi-core architectures**
- **Increased productivity by 3 to 4 times**
- **Reduction in portability and maintenance effort**
- **Scalability up to 100 cores**

#### Model-based Use Case Applications in ARGO

- **Aerospace:** Enhanced Ground Proximity Warning System (EGPWS) from DLR
- **Automation:** Polarization camera POLKA from Fraunhofer IIS
- **Image processing for industrial use cases like image-based material analysis**

#### Code Transformations

- **Enhance predictability and parallelizability**
- **Optimized Scheduling**
- **Reduced system (multi-core) execution time (WCET)**

#### Data Management & Synchronization

- **Scalable data management for memories**
- **Uses message & shared memory**
- **Optimized synchronization placement**

### ARGO ADL

- **Hardware information provided by the WCET-aware ARGO Architecture Description Language (ADL)**
- **Front-End Tools**
  - Translate Scilab Code & Xcos Models to sequential C code
  - Generates staticaly analyzable code with annotations for WCET information and back-traceability

### ARGO WCET-Aware Parallelization Tool-Chain

- **Cross-layer optimization in parallelization compilers**
- **Optimized Schedule & Mapping using WCET metrics**
  - Different algorithms to tweak the trade-off between performance and solution quality
  - Support heterogeneous platforms by considering ADL information
- **Reduce the gap between worst-case and average-case performance**
- **Tightly estimate worst-case execution time (WCET)**

### ARGO Target Hardware Platforms

- **InvasIC Architecture**
  - InvasIC = „Invasive computing”
  - Academic heterogeneous, tiled multi-core architecture
  - LEON3 cores with tile-local memory
  - Deterministic Network-on-Chip (NoC)
  - Parameterizable to ensure WCET analyzability (e.g. disabled caches)

- **FlexaWare Architecture**
  - Platform for real-time streaming analytics
  - Parallel data streams feed right into the processor network
  - 200+ RISC processor cores and optimized hardware accelerators
  - Heterogeneous with NUMA
  - Low-latency local memories in a distributed memory architecture

### ARGO Project Partners


### References