WCET-Aware Parallelization of Model-Based Applications for Heterogeneous Parallel Systems

Challenge: Parallel programming of heterogeneous multi-core systems with time-critical embedded applications

Approach: WCET-aware automatic parallelization and tool-based user-guided parallelization with guaranteed real-time constraints

OBJECTIVES

WCET-aware automatic parallelization

WCET-analysis for heterogeneous multi- and many-core architectures

Cross-layer programming user interface

Model-based development and testing

EXPECTED IMPACTS

Productivity increase and reduction of time-of-market

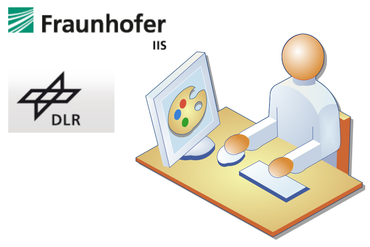
Reduction in portability and maintenance effort

Maximizing worst-case speedup by using multiple cores

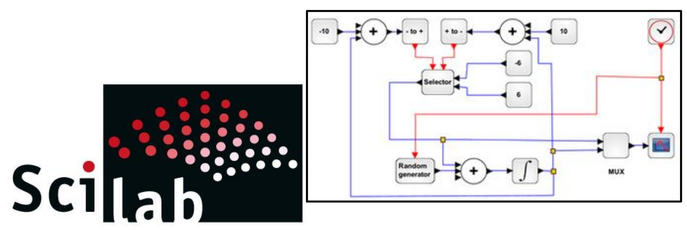
Reducing the gap between worst- and average-case performance

Scalability up to 100 cores

Proof of concept for aerospace and automation domain applications



Application Test Cases

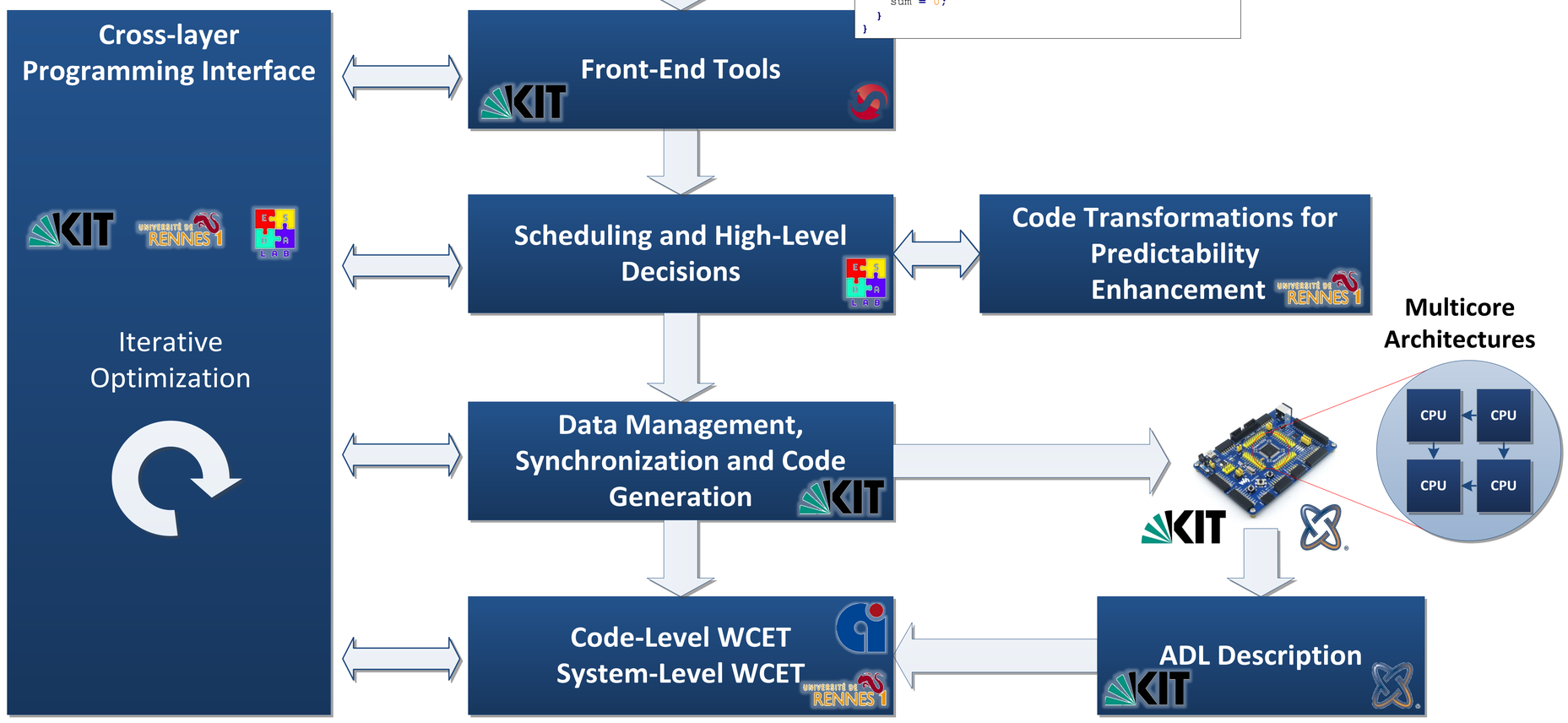


Xcos / Scilab Application Models

Feedback & Control

```
int m, n, p, q, c, d, k, sum = 0;
int first[10][10], second[10][10], multiply[10][10];


for (c = 0; c < m; c++) {
  for (d = 0; d < q; d++) {
    for (k = 0; k < p; k++) {
      sum = sum + first[c][k]*second[k][d];
    }
    multiply[c][d] = sum;
    sum = 0;
  }
}
```



Application Test Cases

- **Aerospace:** Enhanced Ground Proximity Warning System (EGPWS) and Wake Encounter Avoidance and Advisory System (WEAA)
- **Automation:** Polarization camera POLKA and multi sensor fusion
- Assessment and prototyping with novel heterogeneous multi- and many-core architectures

Iterative Cross-Layer Optimization

- **Interactive** User Interface to visualize and control Scilab/Xcos model compilation to multi-core under hard real-time constraints
- Access to all layers of abstraction enabling **iterative cross-layer optimizations**
- **Visual** representation of parallelization decisions with input cross-references, e.g. **processor timeline, memory mapping, data movement**
- **Identify** application bottlenecks, processor idle time busy blocks, data transfer patterns etc.

Frontend Tools

- Model-based development of real-time applications with Scilab/Xcos
- Translation into annotated Scilab language
- Provide statically analysable **intermediate representation (IR)**
- Consideration of lower level annotations, e.g. WCET analysis to ensure **traceability**

High-Level Decisions

- Development of **platform independent static scheduling and mapping** algorithms
- Support for heterogeneous platforms by consideration of ADL information
- **WCET-aware** optimization
- Toolbox of different algorithms supports accuracy/performance flexibility

WCET-aware Code Generation

- Use of a generic scheme to describe data movements between parallel tasks
- Minimize worst case communication delays
- Target specific code generation

Code- and System-Level WCET

- Advanced WCET estimation for parallel computation systems
- System level WCET in addition to conventional Code-Level WCET
- System level WCET estimates worst case communication and synchronization times
- **Reducing the gap** between worst- and average-case performance

Code Transformations

- Improving **program predictability** amenable to accurate code-level WCET analysis
- Systematic use of **software controlled scratchpads**
- Data partitioning / layout transformation
- Reducing shared resource conflicts

WCET-aware Architecture Description

- Abstract multi-core description with ADL
- Including **code- and system-level information**
- Comply with cross-layer programming interface
- Provide platform agnostic information to the whole toolchain

ARGO Partners

Karlsruhe Institute of Technology; scilab enterprises; RECORE; Université de Rennes 1; Computer & Informatics Engineering Department, Technological Educational Institute of Western Greece; AbsInt; DLR; Fraunhofer IIS

ARGO

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